AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claim 1 (previously presented) A timing controller comprising:

a first circuit which generates a first delay time to an external clock;

a second circuit which generates a second delay time to an output of said first circuit; and

a time difference expander for expanding a time difference between a first changeover point of an output of said second circuit and a second changeover point of the output of said first circuit to provide an output signal from said time difference expander having an equalized changeover point with respect to said external clock.

Claim 2 (canceled).

Claim 3 (previously presented) A timing controller as claimed in claim 1, wherein said first circuit is an input buffer, and said second circuit is a delay circuit.

Claims 4-13 (canceled).

Claim 14 (previously presented) A timing controller comprising:

a first internal circuit which generates a first delay time to a control signal;

a time difference expander for expanding a time difference between a first changeover point of an output of said first internal circuit and a second changeover point of an output of a specific part of said first internal circuit; and

a second internal circuit which generates a second delay time to an output of said time difference expander, the first changeover point being produced by a cycle of the control signal, the second changeover point being produced by the next cycle of the control signal, a delay time of said second internal circuit being substantially equal to a delay time of the specific part of said first internal circuit.

Claim 15 (original) A timing controller as claimed in claim 14, wherein the control signal is a clock signal.

Claim 16 (original) A timing controller as claimed in claim 14, wherein said timing controller provides an output signal before a rise or fall of the control signal and sustains the output signal for a given period around the rise or fall of the control signal.

Claim 17 (withdrawn) An electric circuit comprising:

a first clock buffer circuit receiving an external clock signal;

a first clock delivery circuit; and

a first clock timing control circuit, being supplied with an output of said first clock buffer circuit and an output of said first clock delivery circuit, for generating a preceding internal clock before the output of said first clock buffer circuit being output.

Claim 18 (withdrawn) An electric circuit comprising:

a first clock buffer circuit receiving an external clock signal;

a first clock delivery circuit;

a first delay circuit for duplicating delay time characteristics of said first clock buffer circuit; and

a first clock timing control circuit, being supplied with an output of said first clock buffer circuit and an output of said first delay circuit, for generating a preceding internal clock before the output of said first clock buffer circuit being output.

Claim 19 (withdrawn) An electric circuit as claimed in claim 18, wherein said first delay circuit duplicates delay time characteristics of said first clock buffer circuit and said first clock delivery circuit.

Claim 20 (withdrawn) An electric circuit as claimed in claim 18, wherein said electric circuit further comprises a first optional circuit, and said first delay circuit duplicates delay time

characteristics of said first clock buffer circuit, said first clock delivery circuit, and said first optional circuit.

Claim 21 (withdrawn) An electric circuit as claimed in claim 20, wherein said electric circuit further comprises a first clock frequency control circuit for receiving an output of said clock buffer circuit, and an output of said first clock frequency control circuit is also supplied to said first clock timing control circuit.

Claim 22 (withdrawn) An electric circuit as claimed in claim 20, wherein said first clock timing control circuit stores capability information into a memory, and the capability information relates to the input from the output of said first clock buffer circuit and the output of said first delay circuit.

Claim 23 (withdrawn) An electric circuit comprising:

a first clock buffer circuit receiving an external clock signal;

a first clock delivery circuit; and

a first clock timing control circuit, being supplied with an output of said first clock buffer circuit and an output of said first clock delivery circuit, for generating an output coincident with said external clock signal.

Claim 24 (withdrawn) An electric circuit comprising:

a first clock buffer circuit receiving an external clock signal;

a first clock delivery circuit;

a first delay circuit for duplicating delay time characteristics of said first clock buffer circuit; and a first clock timing control circuit, being supplied with an output of said first clock buffer circuit and an output of said first delay circuit, for generating an output coincident with said external clock signal.

Claim 25 (withdrawn) An electric circuit as claimed in claim 24, wherein said first delay circuit duplicates delay time characteristics of said first clock buffer circuit and said first clock delivery circuit.

Claim 26 (withdrawn) An electric circuit as claimed in claim 24, wherein said electric circuit further comprises a first optional circuit, and said first delay circuit duplicates a delay time characteristics of said first clock buffer circuit, said first clock delivery circuit, and said first optional circuit.

Claim 27 (withdrawn) An electric circuit as claimed in claim 26, wherein said electric circuit further comprises a first clock frequency control circuit for receiving an output of said clock buffer circuit, an output of said first clock frequency control circuit is also supplied to said first clock

timing control circuit, and said first clock timing control circuit generates an output coincident with a part of said external clock signal.

Claim 28 (withdrawn) An electric circuit as claimed in claim 26, wherein said first clock timing control circuit stores capability information into a memory, the capability information relates to the input from the output of said first clock buffer circuit and the output of said first delay circuit, and said first clock timing control circuit generates an output coincident with a part of said external clock signal.

Claim 29 (currently amended) A timing controller comprising:

a[[.]] first delay circuit receiving a first clock signal and outputting a second clock signal;

a variable delay circuit, receiving the first and second clock signals and delaying the second clock signal, and having a delay time determined by expanding a time difference between a first changeover point of the first clock signal and a second changeover point of the second clock signal; and

a second delay circuit connected to said first delay circuit and said variable delay circuit in series, and thereby said timing controller generates a control clock signal having a given time difference with respect to the first clock signal.

Claim 30 (canceled).

Claim 31 (previously presented) A timing controller as claimed in claim 29, wherein the delay time of said first delay circuit is substantially equal to the delay time of said second delay circuit.

Claim 32 (previously presented) A timing controller as claimed in claim 29, wherein a change timing of the control clock signal is consistent with a change timing of the first clock signal.

Claim 33 (previously presented) A timing controller as claimed in claim 29, wherein said first delay circuit has a delay time corresponding to total delay times of an input buffer, a wiring, and an output buffer.

Claim 34 (previously presented) A timing controller as claimed in claim 29, wherein the delay time of said second delay circuit is shorter than that of said first delay circuit.

Claim 35 (previously presented) A timing controller as claimed in claim 29, wherein the delay time of said second delay circuit is shorter by the delay time of an output buffer than the delay time of said first delay circuit.

Claim 36 (previously presented) An electronic circuit having a timing controller and an output buffer, said output buffer receiving a control clock signal and outputting signal in response

to the control clock signal, said timing controller comprising:

a first delay circuit receiving a first clock signal and outputting a second clock signal;

a variable delay circuit, receiving the first and second clock signals and delaying the second clock signal, and having a delay time determined by expanding a time difference between a first changeover point of the first clock signal and a second changeover point of the second clock signal; and

a second delay circuit connected to said first delay circuit and said variable delay circuit in series, and thereby said timing controller generates said control clock signal having a given time difference with respect to the first clock signal.